R56

Cross Talk, Quantum Efficiency, and Parasitic Light Sensitivity comparison for different Near Infra-Red enhanced sub 3um Global Shutter pixel architectures

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Abstract

This paper discusses enhancement of Near Infra Red (NIR) performance of 2.8um GS pixels.

Introduction

In recent years there is increasing interest in high resolution sensors optimized for the NIR regime, for example 3D mapping using structured light [1]. The demand for mobile NIR sensors is also increasing, which leads to reduction in pixel size. Moreover, these new applications often need synchronization with NIR sources, which leads to Global Shutter (GS) pixels with small fill factor. Since NIR photons have weak interaction with silicon, special optimization techniques are needed. In this paper we will discuss the optimization for NIR on sub 3um GS pixels.
Two different optimization approaches for NIR enhancement are presented. The first method is using ultra deep Boron (>4MeV) and Phosphorus (>7MeV) implants on n-type material. The schematic of the first approach can be examined on Fig.1. The potential of the pinned diode can be examined in Fig.2. It is clear that the diode reaches 6um into the silicon and has good electrical isolation, with strong barrier that prevents electrons to move from illuminated pixel to its neighbors. In this approach the main factor that determines the diode collection depth is the highest Boron energy, which can be materialized in a given process. The high energy Boron implant is used for creating vertical overflow barrier to the n-type substrate, and for creating the pixel to pixel isolation. The width of Boron implanted barriers between adjacent pixels needs to be as narrow as possible since any absorption in that area will cause reduction of Quantum Efficiency (QE), or increase in the cross-talk (X-talk). The second approach is to use thick p-type high resistivity (HR) wafer. The schematic of this approach is illustrated in Fig.3. In Fig.4, the potential diagram is shown. In this approach the collection depth is limited by the initial wafer thickness (and somewhat by the process thermal budget). The HR is used to reduce X-talk, as the pinned diode induced-field acts as an electrostatic lens that directs the generated electrons to the illuminated pixel [2].

X-talk Simulation

Our simulations were performed on a 2.8um GS pixel structure with dual micro lens and w-shield [3,4]. The simulations were done only for 850nm wavelength. On our simulation deck we used extension of the MN w-shield to block the illumination coming to the left pixel. This simulation method helped us to isolate the x-talk components coming from backend to the x-talk, which is caused by the thick silicon and the small absorption of NIR. In Fig. 5 the simulated light intensity in the silicon is shown for 0deg, 5deg , 10deg and 14deg . It is seen that our pixel optics is efficient concentrating the light field below the illuminated pixel up to roughly 4um. From that depth the light field is growing under the covered pixel and will contribute to x-talk. This x-talk is due to optical effect only and not due to electron diffusion, which can degrade the spatial resolution even further. In Fig. 6 we used the simulation results to calculate the expected QE of the illuminated pixel and the x-talk, versus the silicon collection depth. The x-talk is defined here as the ratio between the QE of illuminated pixel to the QE of the covered pixel. We compared two cases, the case of 0deg (large aperture on external lens) and the case of 10deg illumination (real world case with f# 2.8). The simulated x-talk for lower f# and higher incident angle is higher than x-talk for 0deg incident angel. Moreover the degradation with respect to absorption depth is shown to be much higher.

Experimental Results

Four different samples were fabricated using same process for back end: standard diode on n-type with absorption depth of about 3um; deep diode on n-type with absorption depth of about 6um; diode on 9um HR p-type wafer and diode on 12um HR p-type wafer. The spectral response from three different samples can be compared in Fig.7. There is a significant enhancement of the IR response for deep diode versus the standard diode. There is even more significant enhancement when we move to the thick high resistivity integration scheme. The Modulation Transfer Function (MTF) was measured using resolution charts and software from Imatest [5]. Our measurement system is shown schematically on Fig.8. The MTF50 in our system is limited to around 100lpm by our system lens. Our standard diode will typically shows MTF50 of 100lpm up to 900nm. A comparison between the deep diode sample and the p-type substrate high resistivity samples is shown in Fig 9. The deep diode MTF is quite stable up to ~780 and degrades only by 20%in 850nm. The MTF measured on p-type HR samples is degrading very fast starting from ~600nm. This degradation at shorter wavelength is attributed to electrical x-talk coming from absorption of photons in the strongly implanted p-region below the memory node part of the pixel.

Summary

We have shown that increasing the NIR QE of 2.8um GS is possible by using thicker HR wafers. The increase in QE for the HR substrates comes with a price of severe degradation in the MTF. The deep diode MTF at 850nm is only slightly degraded compared to the MTF achieved in the visible. Our simulation shows that for better resolution we will need to focus on improving the light coupling into the pixel especially for higher incident angle. Nevertheless for the deep diode with absorption depth of ~6um we have shown QE of ~20% with only minor degradation of MTF (about 20%) compared to our standard process.

References

[1]http://www.chipworks.com/about-chipworks/overview/blog/inside-the-intel-realsense-gesture-camera [retrieved in January 2017]

[2] A. Lahav, et al., "IR Enhanced Global Shutter Pixel for High Speed Applications", Proc. of 2013 International Image Sensor Workshop, Utah, USA.

[3] M. Tsutsui,et al., "Development of Low Noise Memory Node in a 2.8um Global Shutter Pixel with Dual Transfer", Proc. of 2017 International Image Sensor Workshop, Hiroshima, Japan.

[4] T. Yokoyama, et al., "Design of Double Micro Lens Structure for 2.8um Global Shutter", Proc. of 2017 International Image Sensor Workshop, Hiroshima, Japan.

[5] http://www.imatest.com/

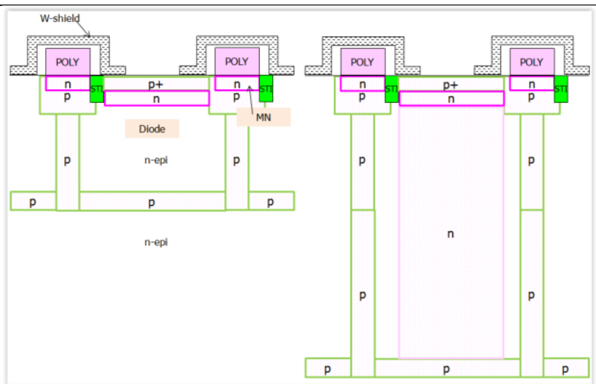

Figure 1 Schematics of standard diode and deep diode on n-type epi wafer

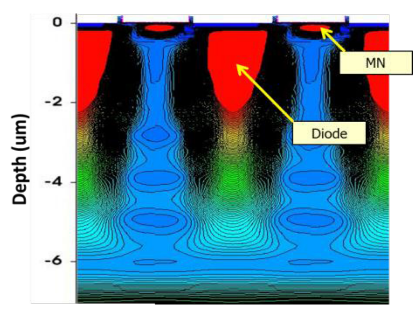

Figure 2 Potential diagram of a deep diode on n-type epi wafer

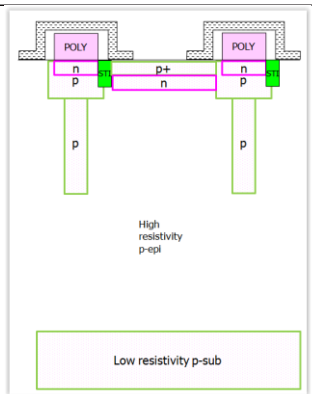

Figure 3 Schematics of diode manufactured on deep p-type high resistivity wafer

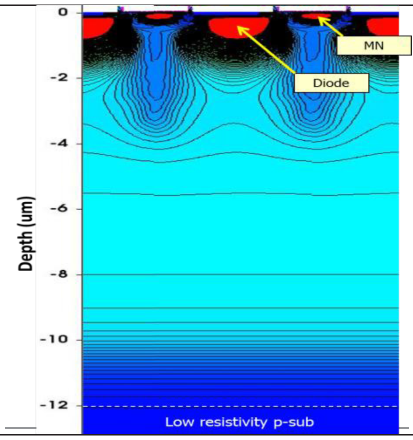

Figure 4 Potential diagram of a diode in high resistivity p-type wafer.

0 deg	5deg	10deg (F#2.8 Max-angle)	14deg (F#2.0 Max-angle)

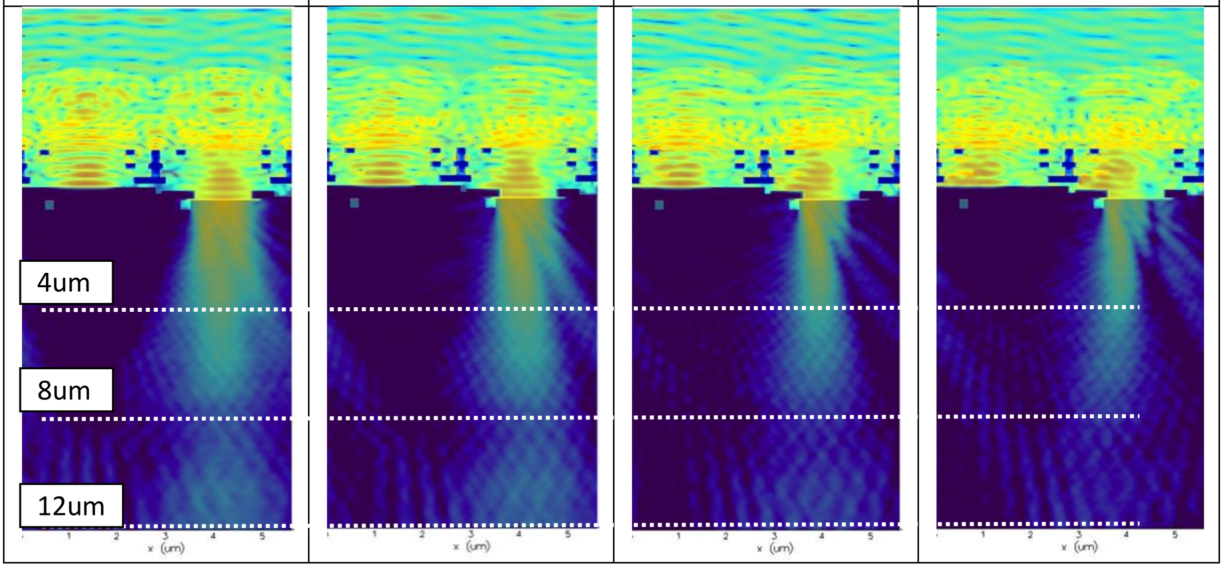

Figure 5. Optical simulation x-section. W-shield is inserted for the left pixel. Different illumination angles are simulated.

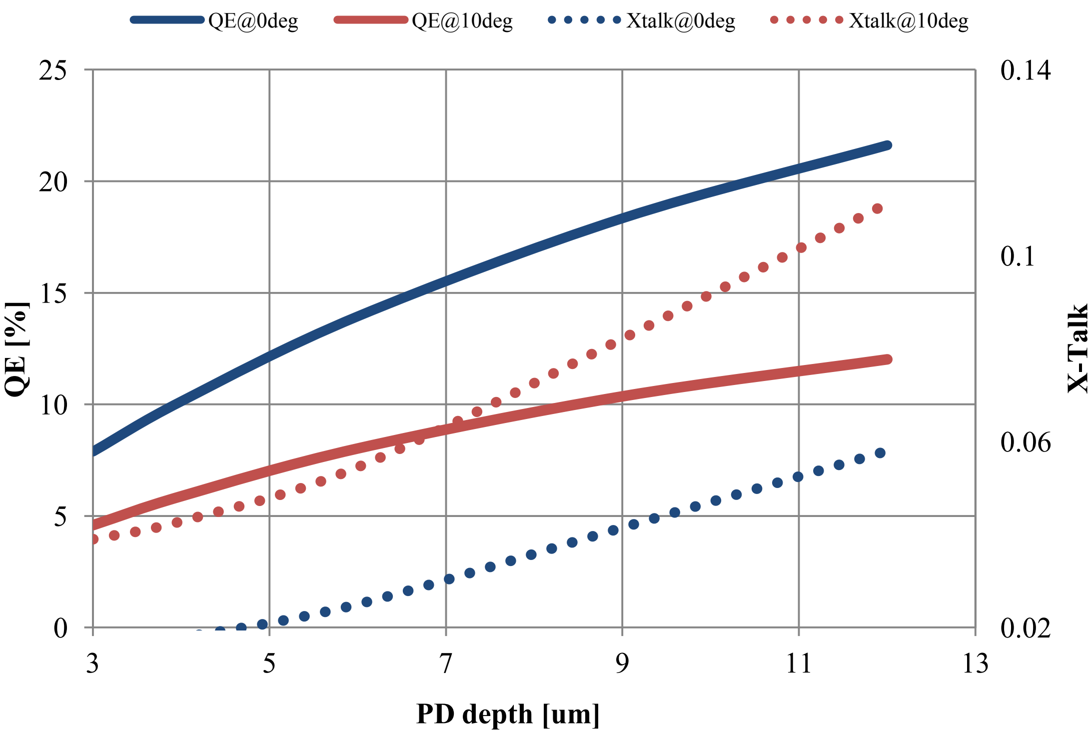

Figure 6 Simulated results of QE and optical X-talk versus absorption depth

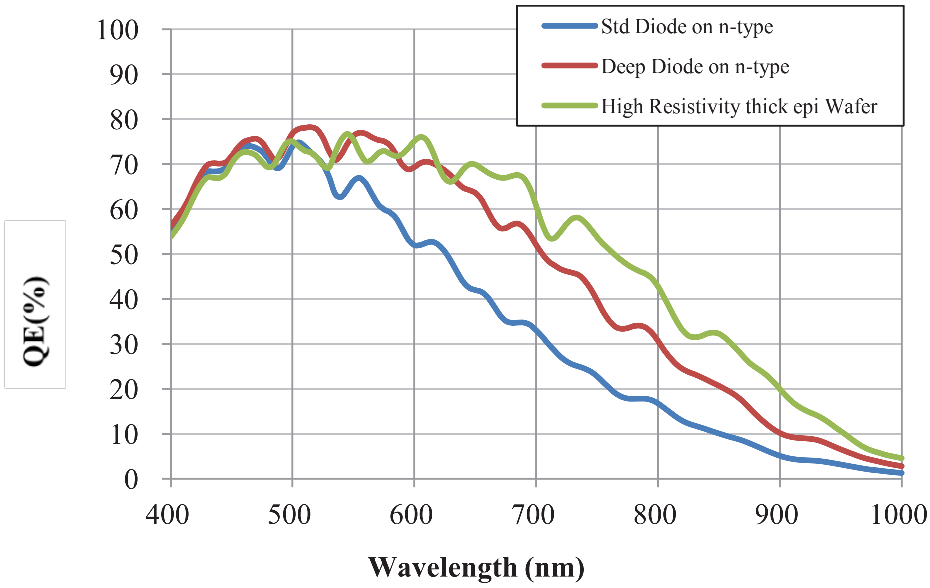

Figure 7 Spectral response for three different pixel integration (Standard, Deep Diode, and 9um HR)

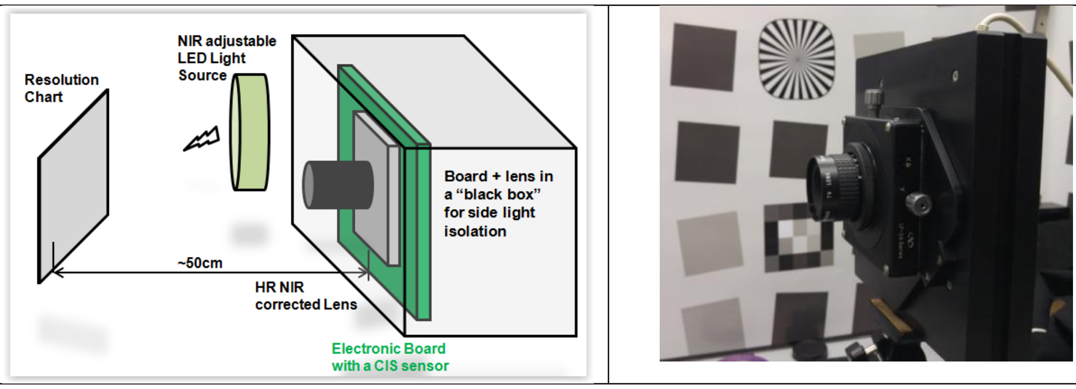

Figure 8 MTF measurement system (resolution charts from http://www.imatest.com/)

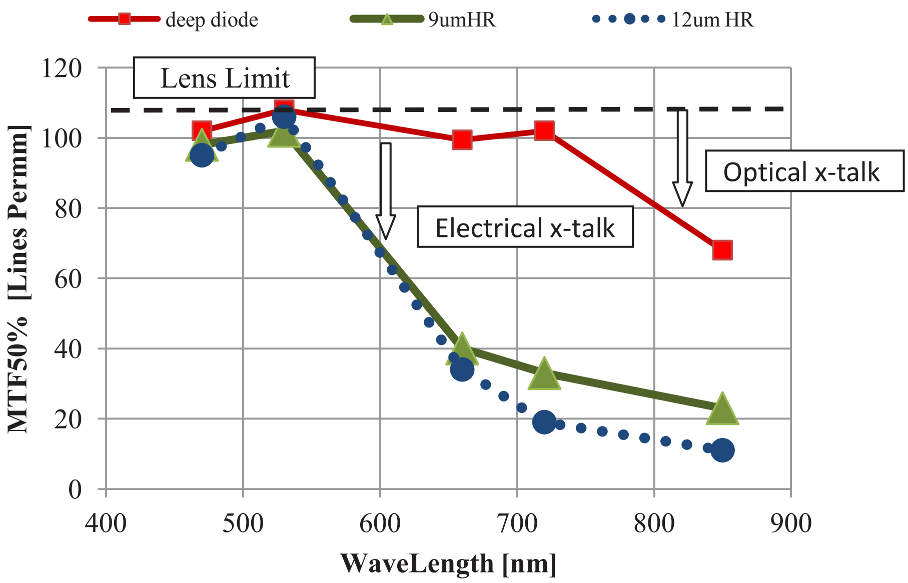

Figure 9 Measurement of the MTF in NIR wavelengths region.